REMARKS

This is in response to the Office Action dated August 17, 2005. Claims 1-10 and 13-19 are pending. Reexamination and reconsideration are respectfully requested.

The Office Action indicates that claims 1, 13 and 14 are allowed and the Office Action rejects claims 2-4, 7-10 and 15-19. Applicant submits that claims 3 and 4 are improperly rejected, because claims 3 and 4 depend from allowed claim 1. Applicant requests correction of this apparent error.

The Office Action objects to claim 2 for its recitation of "common nodes" and suggests that this term should not be plural. Applicant amends claim 2 to address this objection and amends claims 5 and 6 for consistency.

The Office Action rejects claims 2, 5-10 and 15-19 as anticipated by U.S. Patent No. 5,099,148 to McClure, et al. Applicant submits that the claims of the present application distinguish over the McClure patent and are in condition for allowance.

The present application describes a number of input and output circuits that can implement the JEDEC standard input and output characteristics described in the application. Claim 2 relates for example to the circuit illustrated in FIG. 3, which includes first and second unit circuits B1 and B2, each including a pull-up transistor (TP1 and TP2, respectively) and a pull-down transistor (TN1 and TN2, respectively) and each having a common node (C1 and C2, respectively) between their respective pull-up and pull-down transistors and connected through resistors (R11 and R12, respectively) to a single output terminal (OUT). Because two unit circuits are provided with distinct resistors between the unit circuits and the output terminal, output current variations are reduced and there is greater flexibility in designing the performance of the FIG. 3 circuit.

In addition, the two resistors provided along the output current path further limit variations on the output current of the circuit. This is discussed for the FIG. 3 circuit at page 15, lines 1-8 of the present application. Claim 2 reflects this aspect of the disclosure by reciting, "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point."

Applicant submits that claim 2 distinguishes over the McClure patent by reciting the presence of a plurality of unit circuits, as defined by claim 2, with the common nodes of the plurality of unit circuits connected to the single output terminal through first and second resistors. This is not true of the McClure patent. The common nodes identified in the Office Action in the FIG. 1 circuit of the McClure patent *are not connected* to the output terminal D_0. The common nodes are connected to the gates of transistors 12_0 and 14_0 but are electrically insulated from the output terminal D_0. This reflects the fact that the output buffer of the present application operates differently than the buffer circuit of the McClure patent. Claim 2 and its dependent claims distinguish over the McClure patent by reciting the common nodes are connected to the output terminal and are in condition for allowance.

Referring to FIG. 1, the output buffer of the McClure patent includes PMOS transistor 12_0 and NMOS transistor 14_0 connected in series between V_{CC} and ground, with the output terminal D_0 connected between PMOS transistor 12_0 and NMOS transistor 14_0. PMOS transistor 12_0 and NMOS transistor 14_0 each act as switches in this arrangement. When the signal from $PNAND_0$ circuit 20_0 applied to the gate turns PMOS transistor 12_0 on, PMOS transistor 12_0 acts as a pull up transistor to pull the node D_0 to V_{CC} or high. When the signal from $PNOR_0$ circuit 22_0 applied to the gate turns NMOS transistor 14_0 on, NMOS transistor 14_0 acts as a pull down circuit to pull the output node D_0 to 0 V or ground. Signals applied to

the gates of the PMOS transistor 12_0 and NMOS transistor 14_0 cause those transistors to switch and do not reach the output terminal D_0.

Signals applied to the gates of PMOS transistor 12_0 and NMOS transistor 14_0 never reach the output terminal D_0. This is because the gate is *electrically insulated* from the source and drain in each of these transistors. Transistors never act as resistors between their gate electrode and either of the source or drain electrodes.

Turning now to the Office Action, the Office Action states its position that transistors 12_0 and 14_0 are the resistors recited by claim 2. As just discussed, this statement is wrong. A field effect transistor can *never* act as a resistor between its gate electrode and either of its source or drain electrodes. That is the configuration in which the transistors 12_0 and 14_0 are used in the McClure patent's buffer circuit. Consequently, transistors 12_0 and 14_0 cannot function as the resistors claimed by claim 2.

The Office Action's support for the proposition that a transistor "can be a resistor" is claim 10 of the present application. Ignoring the fact that the Office Action is using the present application as prior art against itself, the Office Action errs in not appreciating the specific configuration that must be adopted for a transistor to function as a resistor. Importantly, the field effect transistor can only act as a resistor between its source and drain electrodes. A field effect transistor cannot function as a resistor between its gate and its source and a field effect transistor cannot function as a resistor between its gate and its drain. Consequently, the transistors 12_0 and 14_0 cannot be the resistors of claim 2. As such, claim 2 and its dependent claims 5-10 distinguish over the McClure patent and are in condition for allowance.

Independent claim 15, in pertinent part, recites "first resistors connected respectively between said common nodes of said plurality of unit circuits and a common connecting point of said common nodes." This limitation distinguishes over the McClure patent for the reasons discussed above with respect to claim 2. That is, the McClure patent does not teach the use of resistors between the common nodes and common connecting points in a buffer circuit as defined by claim 15. As such, claim 15 and its dependent claims 16-19 distinguish over the art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4600 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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By: _____
William H. Wright
Registration No. 36,312
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701